

Appl. No. 09/977,069
Amdt. dated May 23, 2003
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PATENT

Amendments to the Specification:

Please add the following paragraphs after the paragraph ending at page 3, line 2 of the specification.

--FIG. 4 shows a cross-section of a device with a diffusion barrier.

FIG. 5 shows a schematic cross-section of a portion of the device shown in FIG.

4.

FIG. 6 shows a schematic cross-section of a circuit structure.--

Please add the following paragraph after the chemical formulas at page 7, line 15 of the specification.

--Embodiments of the present invention provide an integrated circuit comprising a self-assembled monolayer diffusion barrier. FIG. 4 shows an MOS test structure containing a self-assembled monolayer barrier layer. The MOS test structure contains the following elements: a silicon layer 1; a silicon dioxide layer 2 on the top side of the silicon layer; an aluminum back contact 3 on the bottom side of the silicon layer; a diffusion barrier 4 comprising a self-assembled monolayer; and, copper layer 5 deposited on the diffusion barrier. FIG. 5 shows a close-up view of the silicon dioxide layer 2, copper layer 5 and the molecules of the diffusion barrier 4 between the copper layer 5 and the silicon dioxide layer. As shown, aromatic groups 4(a) are in direct contact with the copper layer 5. FIG. 6 shows a cross-sectional view of a circuit comprising a self-assembled monolayer diffusion barrier. The illustrated circuit contains the following elements: a copper layer 6; a self-assembled monolayer diffusion barrier 7 that surrounds the copper layer; and a substrate 8 that includes the copper and diffusion barriers.--